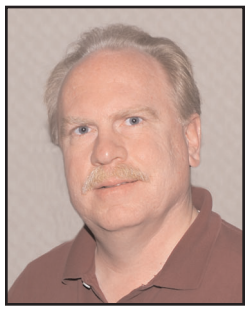
Session 34 Overview

SRAM



Chair: Bruce Bateman, T-RAM, San Jose, CA

Associate Chair: Jinyong Chung, Postech, Pohang, Korea

The demand for SRAM storage is driven by two challenging and often conflicting requirements – the first, being high clock-rate, low latency, and high data-bandwidth for processing and data communications, and the second, being low power for portable battery-powered applications, driving the exploration of extremely low operating voltages on nano-scale process technologies.

Achieving these requirements is made more difficult as process technology scales down to smaller dimensions. Subthreshold leakage currents, gate-oxide tunneling currents, and statistical variations in transistor characteristics make the design of 6T SRAM cells increasingly difficult and solutions tend to increase the memory cell size. Thus, there is a need to find better methods for modeling the electrical characteristics of alternative cell designs and for exploring alternatives to the 6T cell that can offer better density without compromising 6T performance.

The first three papers in this session show advances in the high-performance high-density arena. In Paper 34.1, a 64kB data cache for the POWER6™ processor operating at 5.6GHz in a 65nm SOI process, is described. Cell stability and macro operating power are addressed with the use of dual voltage supplies. A 256kb SRAM block used to build last-level caches in high-performance CPUs is described in Paper 34.2. The 4.2GHz 65nm block uses actively managed dual voltage supplies to reduce power and to provide reliable operation at lower voltages with improved array density. The authors of Paper 34.3 present a 72Mb SRAM with synchronous 144b-wide separate I/Os to achieve a stunning 504Gb/s data bandwidth. The chip offers programmable de-skew and improved input- and output-impedance calibration to assist the board designer in achieving this level of performance.

The fourth paper, 34.4, addresses the need for extremely low power by describing a 256kb SRAM on a 65nm process, operating in the subthreshold regime. A 10T cell design insures subthreshold functionality and low leakage with V_{DD} as low as 0.3V and 0.4V, reducing chip power by 3.8× and 2.4×, respectively, compared to above-threshold operation at V_{DD} of 0.6V.

A new statistical method for determining the write margin of an SRAM cell design is presented in Paper 34.5. The new method takes into account the effects of the feedback in the cell, thus giving a more accurate determination of the cells writability with respect to PVT variation.

The final paper, 34.6, introduces a new thryistor-based memory technology that offers circuit performance similar to SRAM, but at 2× to 3× the density. The technology is demonstrated on a 9Mb test chip on a 0.13μm SOI process with a cell size of only 0.562μm^2, and it scales well to more advanced processes and future technologies such as FinFET.

34.1 A 5.6GHz 64kB Dual-Read Data Cache for the POWER6™ Processor **1:30 PM**

J. Davis, IBM, Poughkeepsie, NY

A dual-read 8-way set-associative data cache comprising four 16kB SRAMs and 2 set-prediction macros per POWER6 core is presented. The array utilizes a 0.75µm² butted-junction split-wordline 6T cell in 65nm SOI. The design features dual power supplies, unidirectional polysilicon, and hierarchical unclamped bitlines for enhanced cell stability and performance.

34.2 A 4.2GHz 0.3mm² 256kb Dual-V_{cc} SRAM Building Block in 65nm CMOS **2:00 PM**

M. Khellah, Intel, Hillsboro, OR

An SRAM macro, implemented in a 65nm CMOS process, uses a dual supply to maximize density while enabling the use of low voltage for the processor core. Measurements of a 256kb block show 4.2GHz operation using 29mW from 1.2V at 85°C, with core logic operating down to 0.7V and a sleep biasing scheme that autonomously compensates for PVT and aging.

34.3 A 72Mb Separate-I/O Synchronous SRAM Chip with 504Gb/s Data Bandwidth **2:30 PM**

C. Tseng, Sony, San Jose, CA

A 72Mb 6T SRAM is designed with 2×144 separate-I/O and random R/W in parallel per cycle running at 875MHz DDR to achieve 504Gb/s bandwidth. It is fabricated in a 90nm CMOS process. Dual R/W self-timed clocks with core emulators are multiplexed to operate the SRAM core at 875MHz. On-chip DLL, programmable I/O skews, and programmable input termination and output driver impedance with precise linearity are essential for this 504Gb/s interface.

34.4 A 256kb Sub-threshold SRAM in 65nm CMOS **3:15 PM**

B. Calhoun, Massachusetts Institute of Technology, Cambridge, MA

A 256kb sub-threshold SRAM operates below 400mV from 0 to 85°C and is implemented in 65nm CMOS technology. For the same 6σ static-noise margin, the sub-threshold SRAM at 0.4V achieves 2.25-times lower leakage power and 2.25-times lower active energy than its 6T counterpart at 0.6V. The SRAM uses a 10T bitcell to enable sub-threshold functionality.

34.5 Redefinition of Write Margin for Next-Generation SRAM and Write-Margin Monitoring Circuit **3:45 PM**

K. Takeda, NEC, Sagamihara, Japan

We redefine write margin in order to be able to quantify the effect of both PVT variation and write-margin improvement. A write-margin monitoring circuit based on this definition is implemented in a 90nm CMOS process. This circuit can be applied to an SRAM power supply circuit to improve the write margin.

34.6 Thyristor-Based Volatile Memory in Nano-Scale CMOS **4:15 PM**

R. Roy, T-RAM Semiconductor, San Jose, CA

A thyristor-based memory cell technology provides SRAM-like performance at 2x to 3x the density of conventional 6T SRAM. The technology is readily embedded into conventional nano-scale CMOS and scales into future SOI and FinFET technologies. A 19mm² 0.13µm 9Mb SOI test chip has a 0.562µm² cell with a cell-R/W time <2ns.